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Hot-Swap MOSFET Application Note

Wide-SOA MOSFET for Hot-Swap Applications

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1. Revision History

Revision	Description	Editor	Date
Rev.01	Initial release	Randy Chiu	2026/10/8

2. Introduction

Inserting a device into a live power system without shutting off the power may generate inrush current, potentially causing system instability or even damage. Hot-Swap circuits and controllers ensure the safety and stability of the power system. In Hot-Swap applications, the design is sometimes limited by the MOSFET SOA (Safe Operating Area), or the system may impose specific inrush current requirements. Conventional Hot-Swap controllers and their peripheral circuits may be unable to meet such requirements, or can do so only at high cost. It is therefore necessary to design an external soft-start circuit tailored to the system requirements.

During soft-start, the pass MOSFET must simultaneously withstand high voltage and high current for several milliseconds—one of the most demanding operating conditions throughout its service life. MOSFETs optimized for high-speed switching applications (e.g., SGT structures with extremely low Q_{GD}) are not necessarily suited to withstanding this linear-mode stress. This application note explains how PANJIT U-Series Wide-SOA MOSFETs fill this gap.

This application note first introduces the basic operating principle, then describes the scenarios in which an external soft-start circuit is applicable, and finally verifies the rationality and feasibility of the external soft-start circuit through experiments. MOSFET selection guidelines are then provided, covering threshold voltage variation, transconductance, SOA, and non-rectangular pulse evaluation, together with measured comparisons.

3. Hot-Swap Circuit Topology

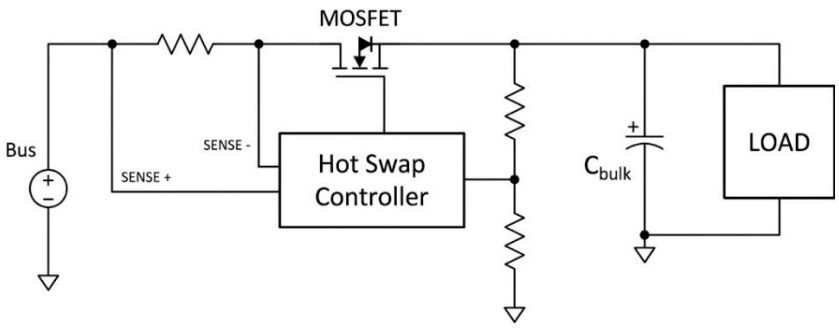


Figure 1. Typical Hot-Swap topology

As shown in Figure 1, the MOSFET is connected in series between the input bus and the bulk capacitor C_{bulk}. The controller senses the current through the sense resistor (SENSE+/SENSE−) and regulates the MOSFET Gate to limit the charging current into C_{bulk}.

4. Hot-Swap Operating Principle

When a device is inserted into the power system, the controller detects the input conditions and drives

the MOSFET gradually rather than turning it fully on at once. This allows the output voltage to rise smoothly while preventing voltage sag in the power system.

During start-up, the MOSFET operates in linear mode, acting as a controlled variable resistor. It limits the inrush current by simultaneously sustaining a high drain-source voltage (V_{DS}) and a high drain current (I_D).

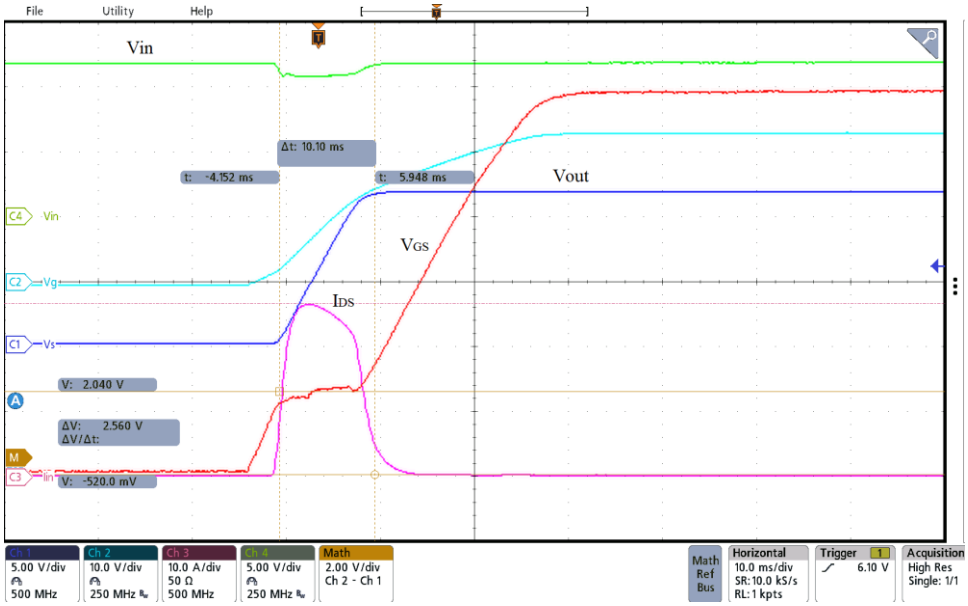


Figure 2. Start-up waveforms

As can be seen in Figure 2, during the 10.10 ms output ramp, V_{GS} remains at the plateau voltage, I_{DS} flows continuously, and V_{DS} gradually decreases from near V_{in}. The MOSFET absorbs the entire start-up energy during this period; therefore, in Hot-Swap design, MOSFET selection is governed by SOA capability rather than by $R_{DS(on)}$.

5. External Soft-Start Design Principle

Taking the LTC4286 typical application as an example:

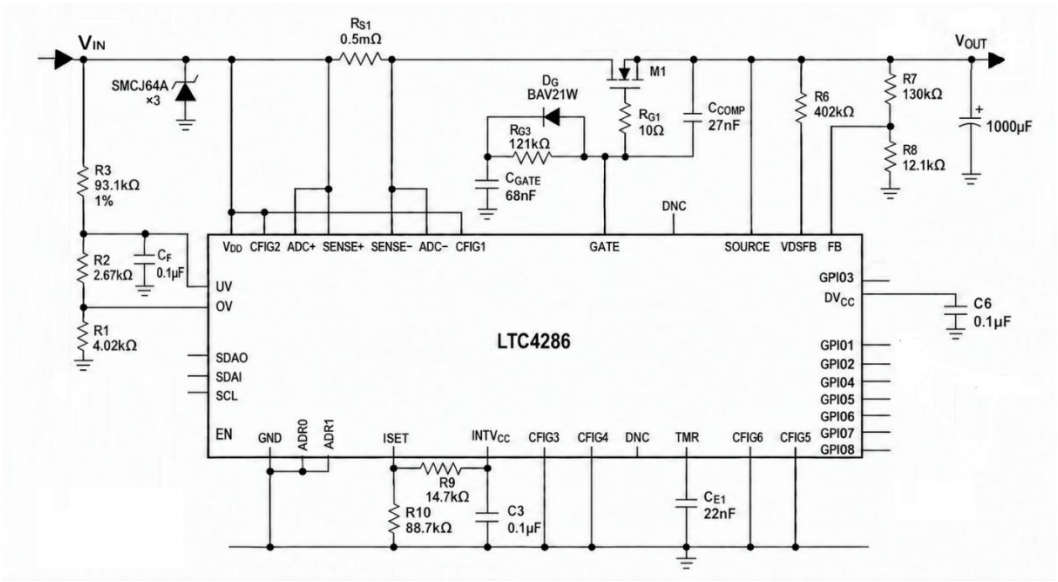


Figure 3. LTC4286 typical application circuit

The MOSFET is turned on by charging the GATE pin with a current source. When the GATE pin voltage reaches the MOSFET threshold voltage, the MOSFET begins to conduct, and the SOURCE voltage then follows the GATE voltage upward. Capacitor C_{GATE} limits the dv/dt of the GATE voltage, thereby controlling the inrush current. The inrush current is given by:

$$I_{INRUSH} = (I_g - nI_{gd}) \times \frac{C_{LOAD}}{C_{GATE}} \quad (1)$$

$$I_{gd} = \frac{dQ_{gd}}{dt} \quad (2)$$

where n is the number of MOSFETs connected in parallel.

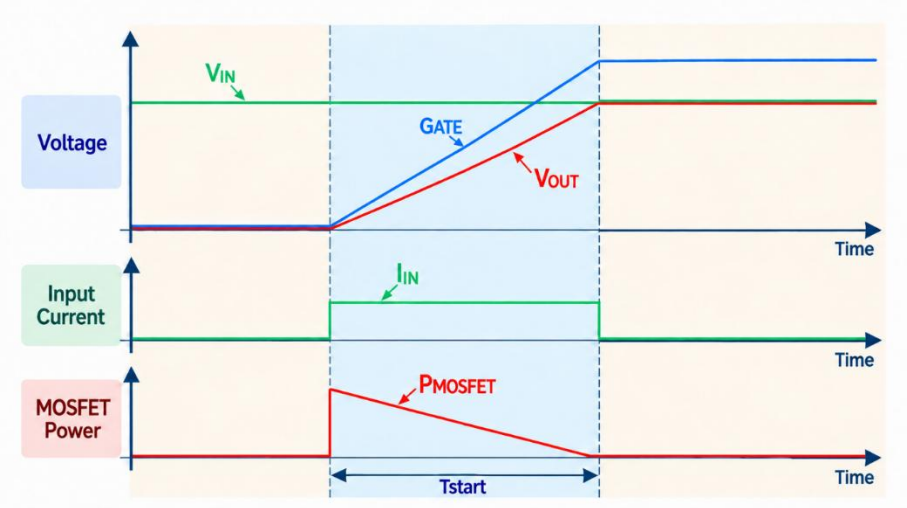


Figure 4. Start-up waveforms with output dv/dt control

Low Q_{GD} is preferred in high-speed switching power supplies; in Hot-Swap applications, however, a larger Q_{GD} actually helps reduce inrush current. Equation (1) explains the mechanism: part of the Gate charging current is diverted by the Gate-to-Drain capacitance of the pass MOSFET. Consequently, a MOSFET with a higher Q_{GD} and C_{rss} effectively provides a built-in "Miller soft-start", which naturally slows the output ramp and reduces inrush current.

As shown in Table 1, the PANJIT U-Series MOSFET PJQ54304UC-AU has a Q_{GD} of 53 nC, larger than the 24 nC of the SGT MOSFET PJQ5514S6C-AU (approx. 2.2×, V_{DS} = 24 V); its C_{rss} is 1063 pF versus 140 pF (approx. 7.5×, V_{DS} = 25 V).

Parameter	Test Condition	PJQ54304UC-AU 30V / 440A $R_{DS(ON)}$ = 0.73mΩ max.	PJQ5514S6C-AU 30V / 525A $R_{DS(ON)}$ = 0.64mΩ max.
C_{iss}	V_{DS}=25V, V_{GS}=0V	13442pF	7402pF
C_{oss}		1193pF	2724pF
C_{rss}		1063pF	140pF
Q_G	V_{DS}=24V, V_{GS}=10V	262nC	122nC
Q_{GS}		25nC	14.5nC
Q_{GD}		53nC	24nC

Table 1. Gate-to-Drain charge comparison of PJQ54304UC-AU and PJQ5514S6C-AU

(Gate charge test current I_{DS}: 50A for PJQ54304UC-AU; 20A for PJQ5514S6C-AU)

6. How to Select the Right MOSFET

When evaluating Hot-Swap MOSFETs, the following four linear-mode criteria should be applied instead of the performance metrics used for high-speed switching applications:

(1) $V_{GS(th)}$ distribution and thermal stability under parallel operation.

(2) Transconductance slope.

(3) SOA capability at the actual V_{DS} and pulse width.

(4) SOA margin under non-rectangular power pulses.

The following sections compare PANJIT U-Series Wide-SOA MOSFETs with conventional SGT MOSFETs against each criterion.

6.1. Impact of Threshold Voltage Variation and the Spirito Effect on Parallel Operation

$V_{GS(th)}$ has a temperature coefficient; during linear-region operation in a Hot-Swap event, $V_{GS(th)}$ decreases as temperature rises. This further increases I_D, forming positive feedback that ultimately leads to thermal runaway (Spirito effect: localized electro-thermal instability of power MOSFETs in linear mode, in which current concentrates at hot spots within the die). Paralleled MOSFETs are particularly vulnerable in linear mode: the device with the lowest $V_{GS(th)}$ turns on first and carries most of the current. Selecting MOSFETs with a consistent $V_{GS(th)}$ distribution and Wide-SOA capability mitigates this issue.

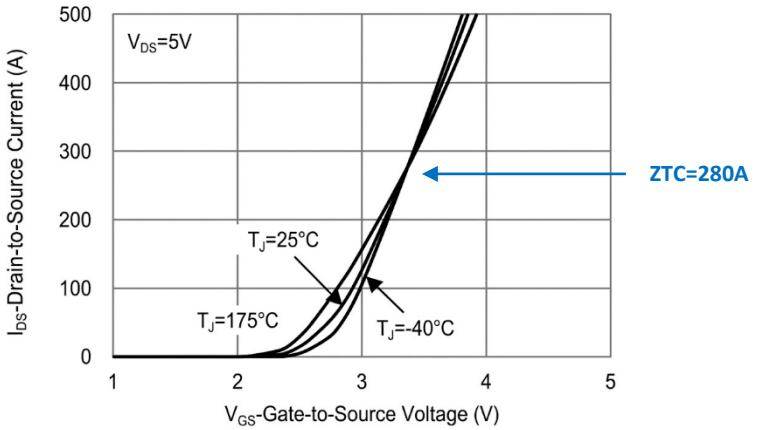


Figure 5. Transfer characteristics of PJQ54304UC-AU

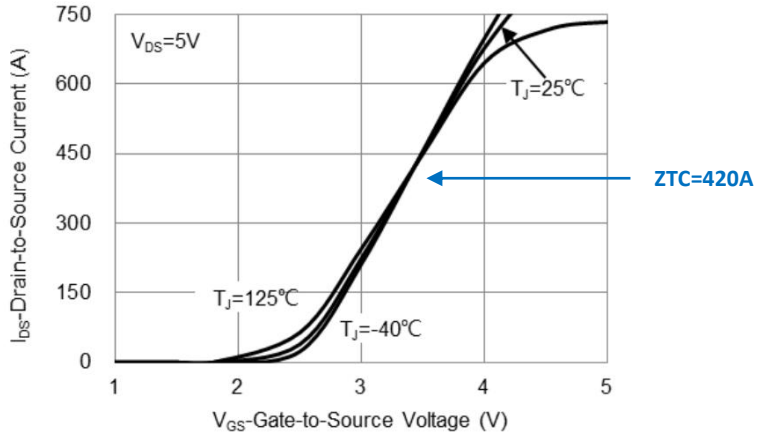


Figure 6. Transfer characteristics of PJQ5514S6C-AU

Below the zero temperature coefficient (ZTC) point, the drain current on the MOSFET transfer characteristic exhibits a positive temperature coefficient. Comparing Figure 5 and Figure 6, the ZTC crossover point of PJQ54304UC-AU is approximately 280 A, whereas that of PJQ5514S6C-AU is approximately 420 A. A lower ZTC current correspondingly shrinks the thermally unstable operating region. This is a key structural advantage of the U-Series.

6.2. MOSFET Transconductance Slope in Hot-Swap Design

$$g_{fs} = \frac{dI_D}{dV_{GS}} \quad (3)$$

A relatively low g_{fs} reduces the sensitivity of I_D to both temperature and voltage variations. For a MOSFET composed of a large number of parallel cells, this results in a more uniform current distribution, reducing the risk of burnout caused by localized overheating.

As shown in Section 6.1, a lower g_{fs} shifts the ZTC point toward lower current, making the die more robust against the Spirito effect during Hot-Swap. Combined with the larger Q_{GD} shown in Section 5, the PANJIT U-Series MOSFET design trades switching speed (which is not critical in Hot-Swap applications) for significantly improved linear-mode ruggedness.

6.3. Ensuring MOSFET SOA in Hot-Swap Design

The SOA diagram is bounded by five limit lines:

- $R_{DS(on)}$ limit line
- Package limit line (peak current limit line)
- Maximum power limit line (green line)
- Thermal instability limit line (red line)
- Breakdown voltage limit line (yellow line)

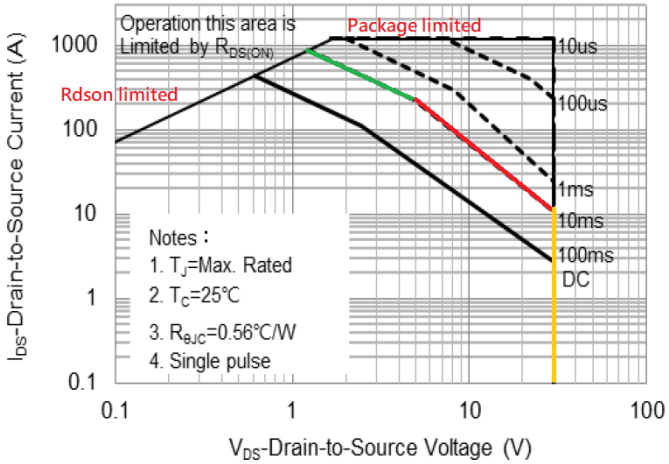


Figure 7. SOA of PJQ54304UC-AU

Region 4, the thermal instability region, is the most critical region. It is difficult to calculate analytically and is best verified through testing.

The SOA diagram shows the relationship among the drain-to-source voltage, the drain current, and the duration for which the MOSFET can sustain that power dissipation. For example, the MOSFET in Figure 7 can withstand 10V and 70A for 10ms; if this condition persists longer, the MOSFET will be damaged. Once the power and duration have been determined, the key requirement is to confirm that the MOSFET

remains within the SOA under all stress conditions.

The derated SOA capability was compared at two pulse widths, 1ms and 10ms; the results are shown in Table 2.

PJQ54304UC-AU, one of the PANJIT U-Series Wide-SOA MOSFETs, demonstrates excellent linear-mode SOA capability in the high-V_{DS}, long-pulse region that dominates Hot-Swap stress.

V_{DS} (V)	t_p (ms)	PJQ54304UC-AU (30V/440A, 0.73mΩ max)	PJQ5514S6C-AU (30V/525A, 0.64mΩ max)	xxx0D55N03CG (30V/462A, 0.58mΩ max)
10V	1ms	>200A	153A	>200A
	10ms	65.15A	37.32A	66.24A
20V	1ms	63.9A	36.35A	78.29A
	10ms	**31.57A**	8.3A	27.02A
30V	1ms	**24.43A**	12.13A	20.24A
	10ms	**13.01A**	6.6A	8.59A

Table 2. Derated SOA capability

Key observations from Table 2:

- **Versus PANJIT SGT MOSFET (PJQ5514S6C-AU):** PJQ54304UC-AU delivers SOA current approximately 1.75 to 3.8 times that of PJQ5514S6C-AU across all test conditions.
- **Versus competitor low-$R_{DS(on)}$ device (xxx0D55N03CG):** PJQ54304UC-AU leads by +16.8% at 20V/10ms, +20.7% at 30V/1ms, and +51.5% at 30V/10ms. At 30V/10ms, this corresponds to a withstand power of approximately 390W versus 258W.
- **PANJIT U-Series MOSFET advantage:** During the initial Hot-Swap period, V_{DS} is close to the full input voltage. In the SOA, the high-V_{DS}, long-pulse corner is dominated by thermal instability — precisely the region where PANJIT U-Series MOSFETs lead by the widest margin.

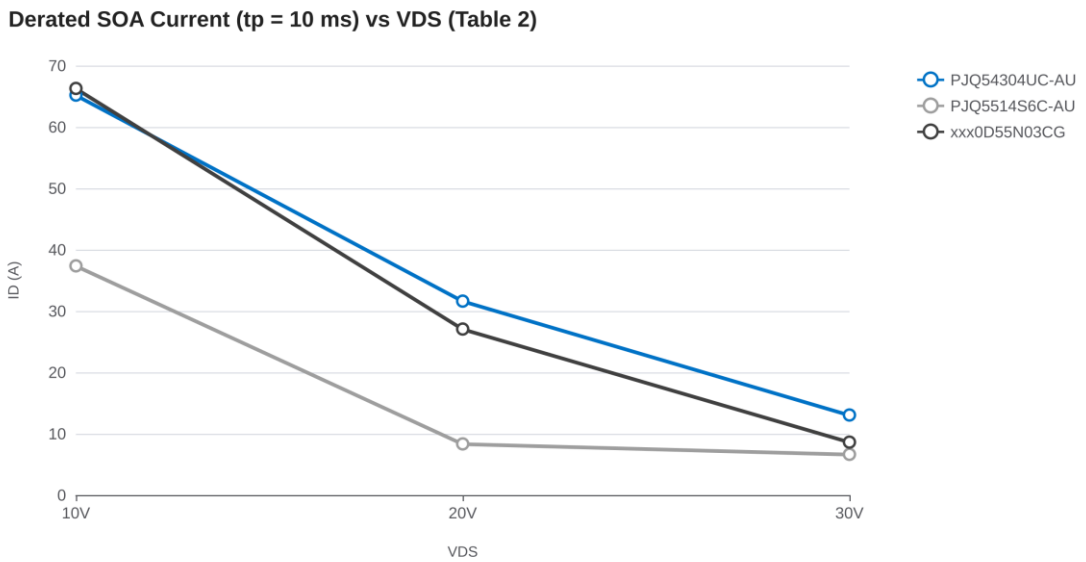


Figure 8. Derated SOA current vs V_{DS} at t_p = 10 ms

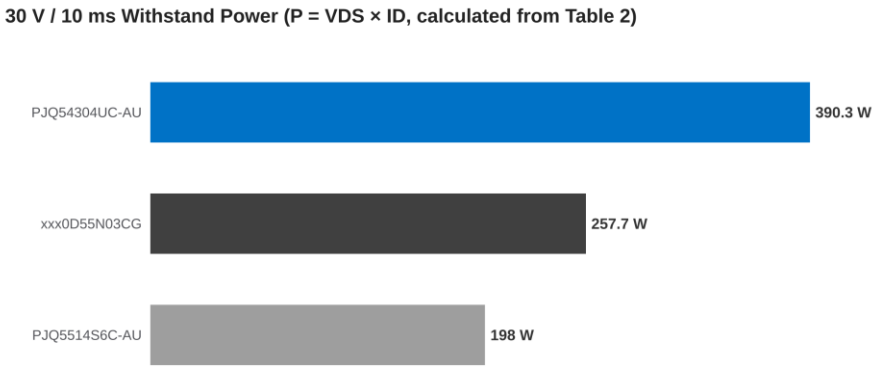


Figure 9. Withstand power at 30V / 10ms, P = V_{DS} × I_D

6.4. SOA Verification for Non-Rectangular Power Pulses

During a Hot-Swap event, the power pulse applied to the MOSFET is not an ideal rectangular pulse but an approximately triangular waveform. When referring to the SOA curves, the triangular power pulse must be converted into an equivalent rectangular pulse.

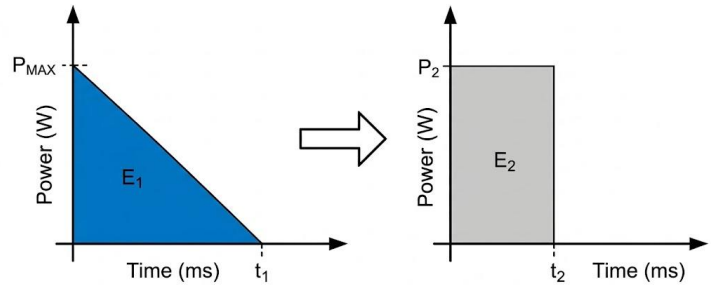


Figure 10. MOSFET stress approximation under non-rectangular pulses

Conversion principle: energy conservation

Assuming V_{DS} is approximately constant, the energy of the triangular pulse (peak current I_{pk}, duration t) and that of the equivalent rectangular pulse are, respectively:

$$E_{triangle} = V_{DS} \times \frac{1}{2} \times I_{pk} \times t \quad (4)$$

$$E_{rect} = V_{DS} \times I_{rect} \times t_{rect} \quad (5)$$

Conversion Form 1: Same peak current, half the duration

$$I_{rect} = I_{pk}\ ;\ \ t_{rect} = \frac{t}{2} \quad (6)$$

On the SOA diagram, use the t/2 curve at I_{pk} to confirm that the operating point lies within the SOA.

Conversion Form 2: Same duration, half the equivalent current

$$I_{rect} = \frac{I_{pk}}{2}\ ;\ \ t_{rect} = t \quad (7)$$

On the SOA diagram, use the curve for duration t at I_{pk}/2 to confirm that the operating point lies within the SOA.

If the maximum current allowed by the SOA diagram at duration t is $I_{SOA,limit}$, then according to Form 2, the maximum allowable peak current of the triangular pulse is 2 × $I_{SOA,limit}$.

7. Conclusion

In Hot-Swap applications, MOSFET selection priorities differ fundamentally from those of high-speed switching applications: SOA, ZTC, and g_{fs} are more important than low $R_{DS(on)}$.

PANJIT U-Series Wide-SOA MOSFETs feature relatively high Q_{GD}、C_{rss} and low g_{fs}. Measured data show that their SOA current is up to approximately 3.8× that of conventional SGT MOSFETs and, at 30V/10ms, up to 51% higher than competitor devices with comparable $R_{DS(on)}$. These characteristics help improve robustness against Hot-Swap inrush stress, reduce potential failure risks, and simplify Hot-Swap design.

The PANJIT U-Series Wide-SOA MOSFET portfolio covers 30V to 100V and fully supports 12V, 24V, 48V, and 54V power systems.

For more product information, please contact our local sales team or visit the PANJIT official website at www.panjit.com

Reference

1) Robust Hot Swap Design / TI
2) MOSFET Selection Guide for Telecom-Server Hot Swap Applications / AOS
3) Linear Mode Operation and Safe Operating Diagram of Power-MOSFETs / Infineon
4) LTC4286 datasheet / ADI

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